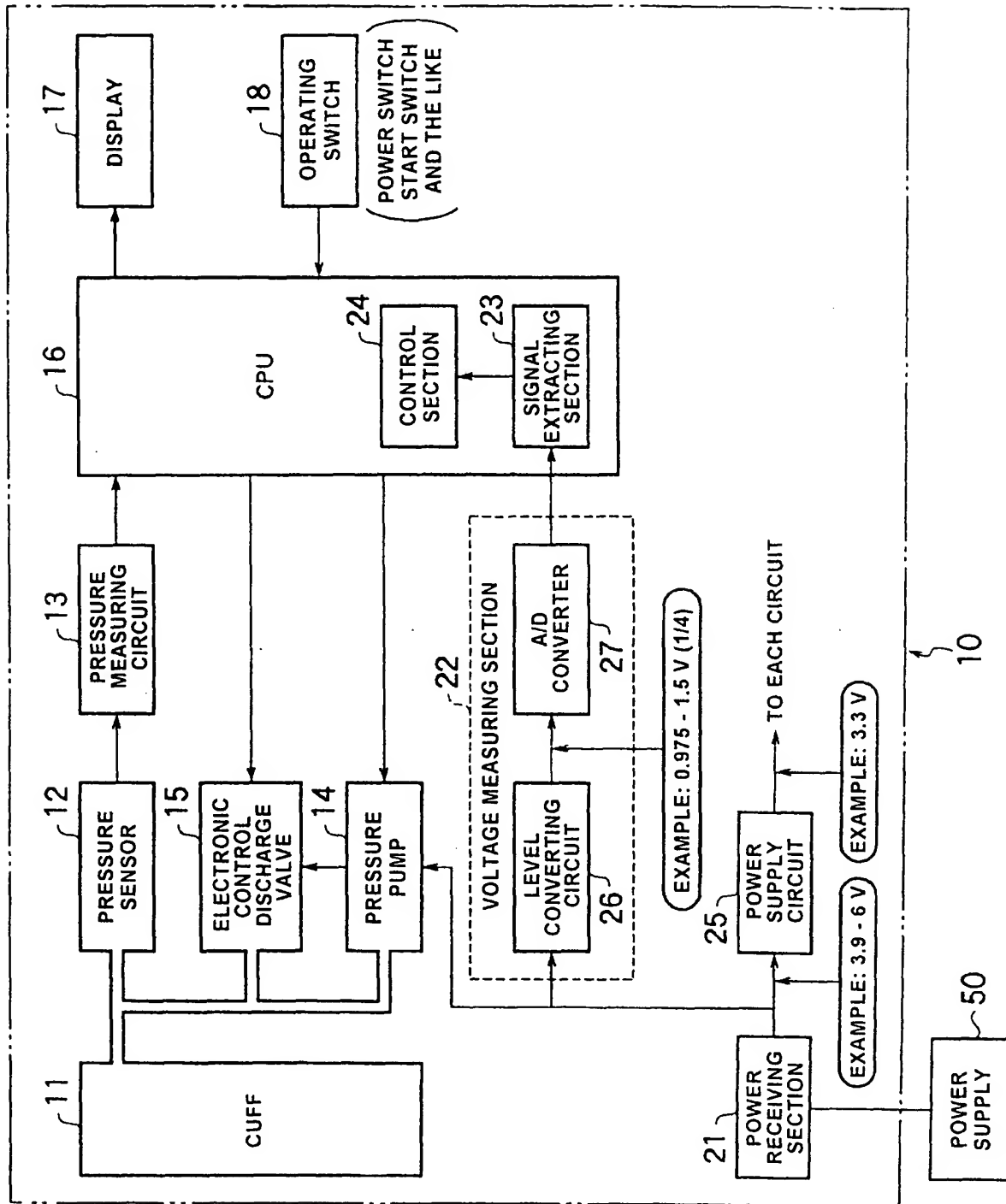


FIG. 1



The diagram shows the output voltage of a DAC over time. The vertical axis represents voltage levels: 0V, MINIMUM OPERATING VOLTAGE, THRESHOLD LEVEL, and RATED VOLTAGE. The horizontal axis represents time, with key events marked: POWER ON, L-LEVEL, DIGITAL CODE, OPERATION TO THE CODE, and DECODING DIGITAL CODE. The output voltage starts at 0V, rises to the MINIMUM OPERATING VOLTAGE, and then settles at the L-LEVEL. It then transitions to the DIGITAL CODE, which is a series of pulses. The output voltage then transitions to the OPERATION TO THE CODE, which is a series of pulses. The output voltage then transitions to the DECODING DIGITAL CODE, which is a series of pulses. The output voltage then transitions to the OPERATION TO THE CODE, which is a series of pulses. The output voltage then transitions to the DECODING DIGITAL CODE, which is a series of pulses.

The diagram illustrates the timing of a digital-to-analog converter. The top trace, labeled "SUPPLIED POWER SUPPLY VOLTAGE", shows a trapezoidal waveform. Horizontal dashed lines indicate the "RATED VOLTAGE", "THLH" (Threshold Level High), "THHL" (Threshold Level Low), and "MINIMUM OPERATING VOLTAGE". The "THLH" level is marked with an arrow pointing to "H", and the "THHL" level is marked with an arrow pointing to "L". The "THLH" level is higher than the "THHL" level. The "MINIMUM OPERATING VOLTAGE" is the lowest level shown. The "RATED VOLTAGE" is the highest level shown. The "SUPPLIED POWER SUPPLY VOLTAGE" trace is divided into vertical segments by vertical lines. The first segment is labeled "Ts". The time axis is labeled "TIME" and has markers for "t1", "t2", and "t12". The "DIGITAL CODE" trace shows a step function that transitions from low to high at "t1" and back to low at "t12". Below the "DIGITAL CODE" trace, there are two callouts: "WHEN GOES HIGHER THAN THLH" and "WHEN GOES LOWER THAN THHL".

FIG.4

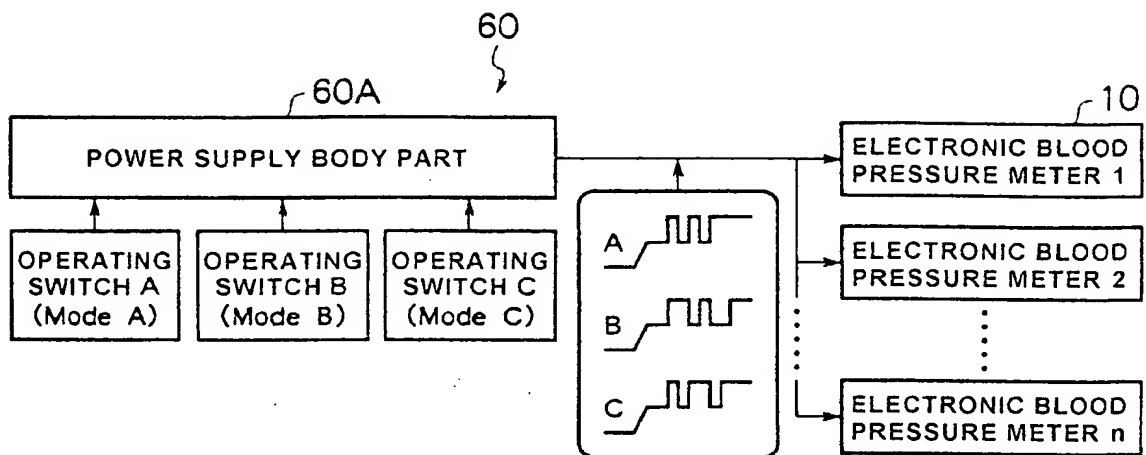


FIG.5

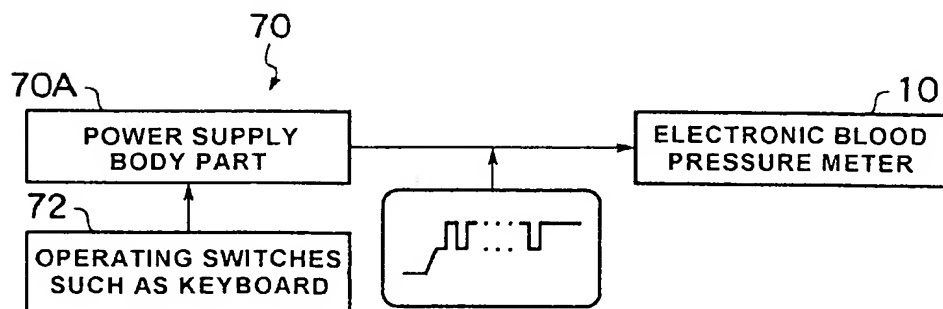


FIG.6

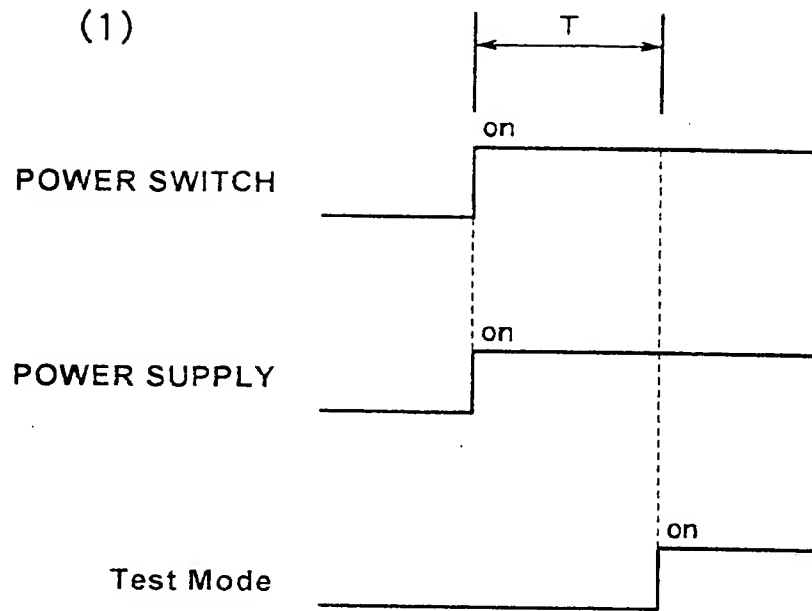


FIG.7

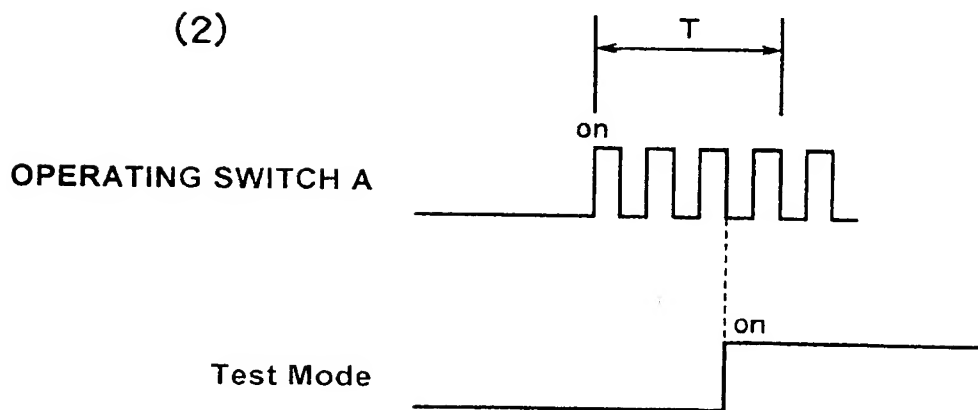


FIG.8

(3)

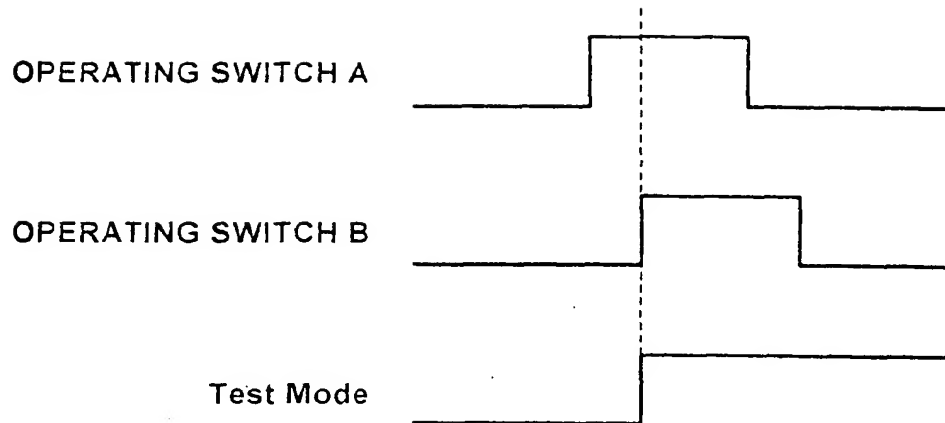


FIG.9

(4)

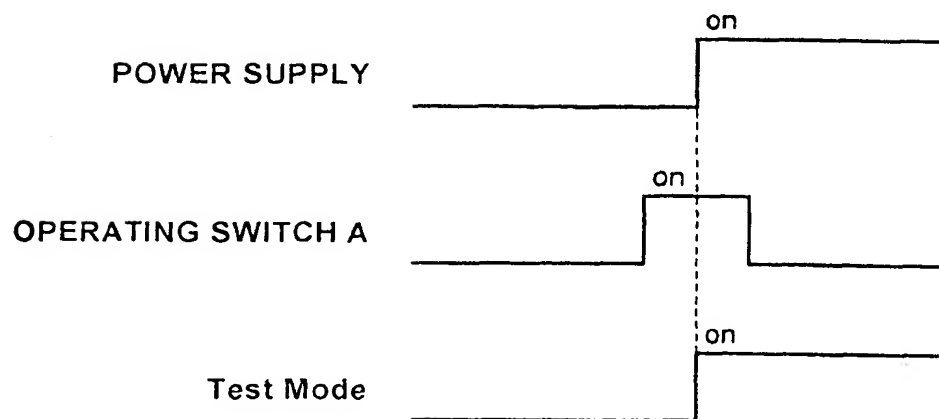


FIG.10

(5)

